REMARKS/ARGUMENTS

Favorable reconsideration of this application, in light of the present amendments and following discussion, is respectfully requested.

Claims 1-17 are pending; Claim 3 and 11 are amended; and no claims are newly added or canceled herewith. It is respectfully submitted that no new matter is added by this amendment.

In the outstanding Office Action, Claim 3 was rejected under 35 U.S.C. § 112, second paragraph; Claims 1, 2, and 4-17 were rejected under 35 U.S.C. § 103(a) as unpatentable over Nagao (U.S. Pat. No. 6,677,674) in view of Kimura et al. (U.S. Pat. No. 6,078,096, hereafter Kimura).

With regard to the rejection of Claim 3 under 35 U.S.C. § 112, second paragraph, that rejection is respectfully traversed. Claim 3 has been amended to address the noted informality. Because Claim 3 stands free of rejections based on prior art, it is respectfully submitted that Claim 3 is now in condition for allowance.

At the outset, Applicant respectfully requests consideration of reference AW previously cited by IDS on February 27, 2004. A copy of the papers as filed, including the date stamped filing receipt, is enclosed herewith. Reference AW was also originally provided by the Applicant in parent application Serial No. 10/190,500, as evidenced by the Examiner's acknowledgement of reference AW in the parent application. Nonetheless, Applicant has provided herewith a courtesy copy of reference AW for the Examiner's consideration.

The present invention, as embodied in the pending claims, relates to a memory chip that is included in a system configured of chips having different functions. In the past, since each type of system required a different memory capacitance, a new memory chip had to be made for every new system. This results in high costs of manufacturing.

Through the claimed invention, various types of memory chips may be obtained from a single wafer, by cutting the chips from the wafer in different ways. In other words, the memory capacitance of a memory chip may be changed by changing the way of the memory chip as cut from a wafer (see, e.g., Figure 5). Additionally, the basic memory chips are not linked with one another by a circuit located inside a dicing line. More specifically, as recited in Claim 1, each basic chip functions as a chip independently from each other basic chip.

With respect to the rejection of Claims 1, 2, and 4-17 under 35 U.S.C. § 103(a) as unpatentable over Nagao in view of Kimura, that rejection is respectfully traversed.

As admitted in the outstanding Office Action at pages 2-3, Nagao does not disclose or suggest the claimed configuration. The outstanding Office Action attempts to remedy this admitted deficiency by relying upon Kimura.

Kimura relates to redundancy technology, which seeks to solve defects in a memory cell array. According to Kimura, only one type of memory chip (with a fixed memory capacitance) may be taken from a wafer. For example, Figure 2 of Kimura illustrates that only one type of memory chip, a 16 Mbit DRAM chip (four 4 Mbit DRAM chips) may be taken out of one wafer because there is already a predetermined way for cutting the wafer. As yet another example, Kimura describes in Figure 8 that only an 8 Mbit DRAM chip (two 4 Mbit DRAM chips) may be taken from one wafer, as a result of the predetermined way of cutting a wafer.

Additionally, Kimura describes a memory chip cut from the wafer that includes basic chips, which are linked with one another by a circuit provided inside a dicing line (interposed between the basic chips). In other words, as illustrated in Figure 9, for example, of Kimura, the basic chips function in connection with each other.

Accordingly, as neither Nagao nor Kimura, either alone or in combination, discloses or suggests that each of the basic chips is operated independently of the other basic chips, it is

respectfully submitted that Claim 1 patentably distinguishes over the applied combination of Nagao and Kimura. It is therefore respectfully requested that this rejection be withdrawn.

Moreover, it is respectfully submitted that there is no basis in the teachings of either Nagao or Kimura to support the applied combination. Certainly, the Office Action fails to cite to any specific teachings within either reference to support this combination. It is therefore respectfully submitted that the combination of Nagao and Kimura is improperly based upon hindsight reconstruction.

Consequently, in view of the foregoing discussion and present amendments, it is respectfully submitted that this application is in condition for allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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Docket No.. 249344US2S DIV

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Yukihiro URAKAWA

SERIAL NO: New DIV Application GAU:

FILED: Herewith EXAMINER:

FOR: MEMORY CHIP AND SEMICONDUCTOR DEVICE USING THE MEMORY CHIP AND MANUFACTURING METHOD OF THOSE

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:
Applicant(s) wish to disclose the following information.

REFERENCES

■ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references were provided in previously filed U.S. Application No. 10/190,500, filed 07/09/2002.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.

☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.

☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

■ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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Form PTO 1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT

ATTY DOCKET NO.	SERIAL NO.
249344US2S DIV	New DIV Application
APPLICANT: Yukihiro URAKAWA	
FILING DATE: Herewith	GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	6,078,096	06/2000	KIMURA, et al.			
	AB	6,372,554	04/2002	KAWAKITA, et al.			
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES	TRANSLATION NO
	AO					
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	Tadahiko SUGIBAYASHI, et al., "A 1Gb DRAM for File Applications", ISSCC DIGEST OF TECHNICAL PAPERS, 1995, pages 254-255
	AX	
	AY	
	AZ	☐ Additional References sheet(s) attached

Examiner	Date Considered

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

E

Dept.: E/M

OSMM&N File No. 249344US2S DIV By: EHK/KDP/dmr

Serial No. New DIV Application

In the matter of the Application of: Yukihiro URAKAWA

For: MEMORY CHIP AND SEMICONDUCTOR DEVICE USING THE MEMORY CHIP AND MANUFACTURING METHOD OF THOSE

Due Date: February 27, 2004

The following has been received in the U.S. Patent Office on the date stamped hereon:

- 35 pp. Specification 17 Claims/Drawings 16 Sheets and 2 Pages Application Data Sheet
- Combined Declaration, Petition & Power of Attorney 2 Pages (copy)
- Utility Patent Application Transmittal
- Request for Priority
- Credit Card Form for $770.00
- Dep. Acct. Order Form
- Fee Transmittal Form
- Information Disclosure Statement
- PTO-1449
- White Advance Serial Number Card

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FA 14.6: A 1Gb DRAM for File Applications

Tadahiko Sugibayashi, Isao Naritake, Satoshi Utsugi, Kentaro Shibahara, Ryuichi Oikawa, Hidemitsu Mori, Shouichi Iwao, Tatsunori Murotani, Kuniaki Koyama, Shinichi Fukuzawa, Toshiro Itani, Kunihiko Kasama, Takashi Okuda, Shuichi Ohya, Masaki Ogawa

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A number of large-capacity DRAMs recently have been developed for file applications because data storage devices play an important role in high-speed communication and graphic systems [1,2]. Such file memories must have low power dissipation, high data transfer rate and low cost. A low chip-yield problem is reported to occur in the manufacture of large capacity DRAMs [3]. To address both device requirements and yield limitations, new circuit technologies are developed for 1Gb DRAMs. By implementing a time-shared offset cancel sensing (TSOCS) scheme and adopting a diagonal bit-line (DBL) cell, the chip size is reduced to 70% of that of a conventional DRAM. A defective word-line Hi-Z standby (DWHS) scheme and a flexible multi-macro (FMM) architecture produces about twice the yield as that resulting from conventional architecture. 32b I/Os with a pipeline circuit technique realizes a 400MB/s data transfer rate. A 1Gb DRAM with these features uses 0.25μm CMOS.

Figure 1 shows the TSOCS circuitry and the timing chart. The conventional offset cancel sensing (OCS) scheme produces a small chip because the number and size of sub-sense amplifiers (SSA) can be reduced [4]. In the DRAM with the TSOCS scheme, since four pairs of bit-lines are connected to one SSA, the number of SSAs is only 25% of that in the DRAM with the conventional OCS scheme. This reduces the SSA area on the chip by approximately 50%. Although the TSOCS scheme restricts random access, only serial block access is needed for most file applications. When the DRAM is activated, bit-line precharge signal (PS) is set to GND level, and then four pairs of bit-lines are discharged to the offset cancel voltage line, OCV, through diode connection (M3 and M4 turn on) of the sense transistors, M1 and M2. The threshold voltage difference between the sense transistors is registered as the bit-line level difference. After this compensation operation, bit-line-separation gates are set to GND level except TG0 connected to the first access bit-line, and then memory cell data are read out to the bit-lines. Sense transistors discharge the main bit-line (MBL) depending on the bit-line voltage level which includes the compensation result. Before the second, the third and the fourth read operations, the bit-lines at the side of the SSA are precharged through the MBL. Since these voltage levels are not compensated, offset cancel signal, OS, is activated, and then the SSA is connected to the bit-lines which retain the compensation voltage level.

The DBL cell is used in the DRAM (Figure 7). The effective cell size is $6.3F^2$, which is smaller than the $8F^2$ of a conventional folded-bit-line cell (F is the feature size) [5]. The DBL configuration features an open bit-line architecture with the disadvantage of array noise impact on the bit-line signal. The array noise has time-damped characteristics. The array noise impact is not critical for file memories because waiting for damping the noise delays only the first access time and precharging time. Figure 2 shows the array noise of a conventional open-bit-line DRAM and the DRAM with the TSOCS scheme just after starting time of a rewrite operation. The TSOCS scheme suppresses the peak of the array noise down to 33%.

The ratio of standby-current fault chips to all manufactured chips is estimated to be approximately 30% for 256Mb DRAMs [2]. Although the conventional replacement redundancy technique increases chip yield, it degrades the cost per-bit of DRAMs because it requires large replacement cell area. File systems use the file allocation table (FAT) which registers fault cluster addresses. The DWHS scheme cuts off standby current faults and only requires 0.4% chip area overhead with 0.1% memory space overhead for the FAT.

Figure 3 shows the 64Mb sub-array block diagram of the 1Gb DRAM and the row decoder circuitry. One fuse is placed in each two main-word decoders (MWD). When a short circuit between the word-line and bit-line exists, the fuse connected to the faulty main word-line is blown out during a wafer probing test at the fabrication stage. A pair of complementary main word-lines, MWL and MWL-bar, are set to GND level and sub-word-lines (SWL) are set to a high impedance state by blowing the fuse in the MWD. Since SWLs at a high impedance state increase the array noise, they are set to GND level by the block select signal, BSL, during the block active period. When the DRAM is used with the DWHS scheme, the roll-call test must be performed with the results sent to the FAT just after power on. In the roll-call test mode, the roll-call signal, RCX, is discharged when an MWD with a blown fuse is selected.

Power supply line or peripheral control circuit faults cannot be repaired by any redundancy scheme, but this fault rate is estimated to be approximately 50% in 256Mb DRAMs [2]. The FMM architecture is developed for chip yield enhancement, as shown in Figure 4. A 1Gb DRAM consists of four 256Mb flexible macros. Flexible scribe lines that include only inter-macro signal lines and device check patterns are laid out between the macros. Because the role of each macro is decided freely by the fuse option, the final scribe line can be moved for higher yield.

Since a macro before the activation of the macro-connection signal (MC) can be used as a 256Mb DRAM, almost all wafer probing tests can be performed as for 256Mb DRAMs. Depending on these test results, the MC and the macro identification signals (MI0 and MI1) are activated by fuse blowing operations. Figure 5 shows the block diagram and circuit diagram of an address path in the DRAM. The third buffer (B3) is placed at each corner of the macro. The MC, MI0 and MI1 selectively activate one buffer that is located at the chip center, and the signals outputted from the other buffers are set to a high-impedance state to prevent short-circuit current caused by dicing.

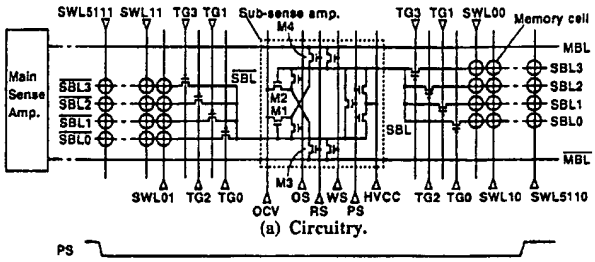
Figure 6 shows the yield of the 1Gb DRAM with FMM architecture, calculated by Monte Carlo simulation. Y_m and Y_0 are the yields of 256Mb macro and the yield of the 1Gb DRAM, respectively. At Y_m=0.5 and using 8-inch wafers, Y_0 is approximately twice that of conventional 1Gb DRAMs.

A 1Gb DRAM uses the proposed circuitry and 0.25μm CMOS. Figure 7 shows micrographs of the full chip which measures 936mm², the chip center, and an SEM photograph of the DBL cells, and measured waveforms. The DRAM has a 2% area overhead due to the FMM architecture. The cell is 0.54μm². The power supply voltage is 2.0 - 2.5V. The clock frequency is 100MHz. I/O pins, address pins and command pins are multiplexed. The first access takes 15 clock cycles. The operating current is 68mA at 2V and 100MHz.

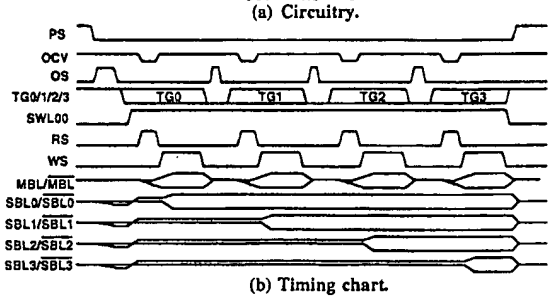
Acknowledgments

The authors express appreciation to K. Okada, I. Sasaki, M. Takada, N. Endo, A. Ishitani, and many colleagues for encouragement and support.

0-7803-2495-1 / 95 / $4.00 / © 1995 IEEE



(a) Circuitry.



(b) Timing chart.

Figure 1: Time-shared offset-cancel sensing scheme: (a) circuitry, (b) timing chart.

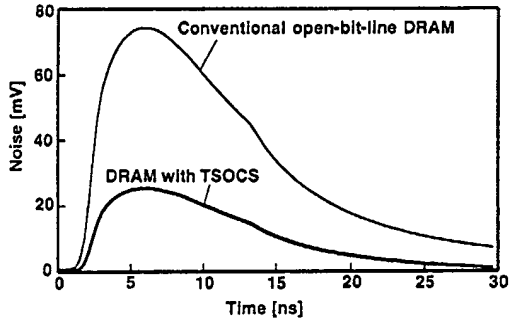
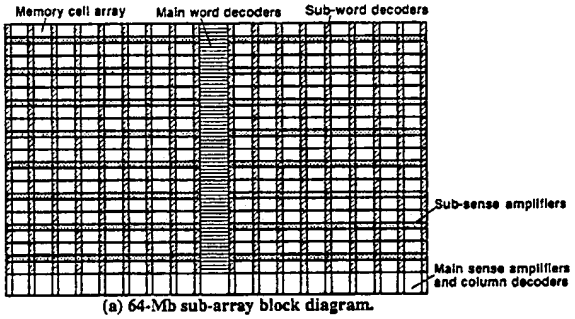
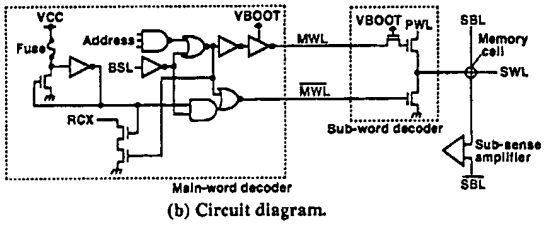


Figure 2: Simulated bit-line waveforms.

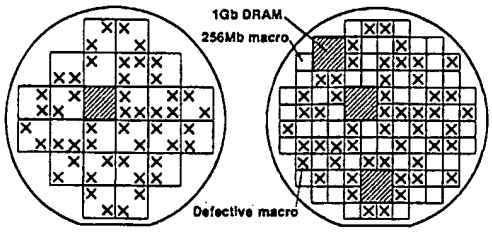


(a) 64-Mb sub-array block diagram.



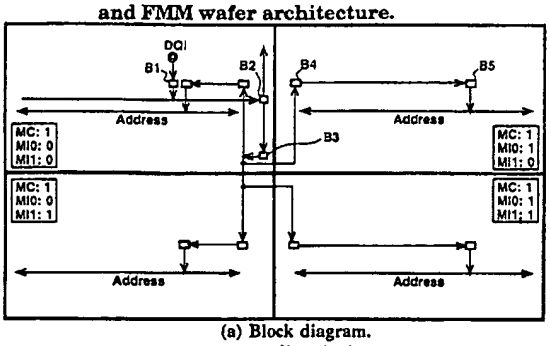
(b) Circuit diagram.

Figure 3: Row decoder circuits.

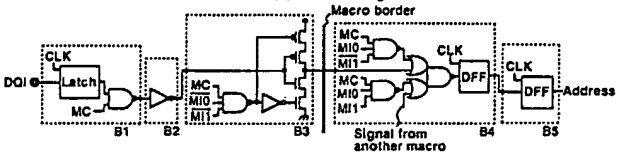


(a) Conventional 1-Gb DRAM wafer (b) wafer of 1-Gb DRAM with FMM architecture

Figure 4: Comparison between conventional DRAM and FMM wafer architecture.



(a) Block diagram.



(b) Circuit diagram.

Figure 5: Address path with FMM architecture.

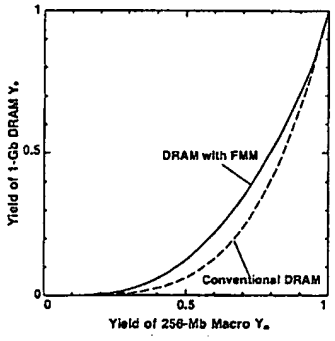


Figure 6: 1Gb DRAM yield.

Figure 7: See page 375.

References

[1] Hasegawa, T., et al., "An Experimental DRAM with a NAND-Structured Cell", IEEE J. Solid-State Circuits, vol. 28, pp. 1099-1104, Nov. 1993.

[2] Kitsukawa, G., et al., "256-Mb DRAM Circuit Technologies for File Applications", ibid, pp. 1105-1113, Nov. 1993.

[3] Komiya, H., "Future Technological and Economic Prospects for VLSI", ISSCC Digest of Technical Papers, pp. 16-19., 1993

[4] Kawahara, T., et al., "A Small-Area, High-Speed, Threshold-Voltage-Mismatch Compensation Sense Amplifier for Gb-Scale DRAM Arrays", Proc. ESSCIRC, pp. 135-138, 1992.

[5] Shibahara, K., et al., "1GDRAM Cell with Diagonal Bit-Line (DBL) Configuration and Edge Operation MOS (EOS) FET", IEDM 1994.